REMARKS/ARGUMENT

Claims 9-22 are now presented for examination. Claim 20 has been amended. Claims 9 and 20 are the only independent claims.

Claim 20 was rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent 5,668,755 (Hidaka et al.). Claims 9-15, 19 and 22 were rejected under 35 U.S.C. § 103 as obvious from Hidaka et al. in view of U.S. Patent 5,571,735 (Mogami et al.). Applicant submits that independent claims 9 and 20 are patentable over the cited prior art for at least the following reasons.

When an inversion bias is applied to a gate electrode of a MOS structure, a depletion region grows in the semiconductor channel region from the interface with the gate oxide film. When the doping level of the gate electrode is light, a depletion region also grows in the poly-silicon gate electrode from the interface with the gate oxide film. The depleted region works like an insulator region, and increases the gate oxide breakdown (durable) voltage. Even when the gate oxide film is thin, the gate electrode with a depleted region can endure a higher voltage. The invention defined by the independent claims provides high voltage CMOS doped at a low impurity concentration to provide enhanced gate oxide breakdown voltage.

Amended claim 20 is directed to a method of manufacturing a semiconductor device. The method comprises: (a) doping an active region and gate electrode of a high voltage CMOS circuit at a low impurity concentration; and (b) doping an active region and gate electrode of a low voltage CMOS circuit at a high impurity concentration after the step (a), to provide a high voltage CMOS circuit having enhanced gate oxide breakdown voltage due to a lightly doped gate electrode relative to the low voltage CMOS circuit.

In the rejection of claim 20 based on Hidaka, , the Examiner referred to figures 1-55, which include all the figures of Hidaka, including the prior art, and related text. Column 8, lines 15-67 of Hidaka is cited as teaching the features of claim 20. However, Applicant cannot find any such description in column 8. Column 8 does show that the well contact regions 14b and 16b are heavily doped p^+ or N^+.

However, a heavily doped well contact region is different from the heavily (or lightly) doped source/drain regions and the heavily (or lightly) doped gate electrode, as are now recited in amended claim 20, and does not adjust the depletion layer which determined the breakdown voltage of the CMOS. For at least this reason, amended claim 20 is believed patentable over Hidaka.

Claim 9 is directed to a method of manufacturing a semiconductor device comprising at least first and second MOS transistors. The method comprises: providing a semiconductor substrate having at least first and second active regions of a first conductivity type and at least third and fourth active regions of a second conductivity type opposite to the first conductivity type; forming a gate oxide layer having a first thickness onto at least the first, second, third and fourth active regions; forming an electrode layer of non-doped polysilicon onto the gate oxide layer; patterning the electrode layer to form first, second, third and fourth gate electrodes onto the first, second, third and fourth active regions, respectively; doping the first active region and the first gate electrode with an impurity of the second conductivity type to form a first transistor driven at a first voltage level, the first gate electrode being doped at a first concentration; doping the second active region and the second gate electrode with an impurity of the second conductivity type to form a second transistor to be driven at a second voltage level lower than the first voltage level, the second gate electrode being doped at a second concentration higher than the first concentration; doping the third active region and the third gate electrode with an impurity of the first conductivity type to form a third transistor to be driven at the first voltage level, the third gate electrode being doped at a third

concentration; and doping the fourth active region and the fourth gate electrode with an impurity of the first conductivity type to form a fourth transistor to be driven at the second voltage level, the fourth gate electrode being doped at a fourth concentration higher than the third concentration. The recited structure includes high and low voltage n-channel transistors and high and low voltage p-channel transistors.

Independent claim 9 was rejected in view of Hidaka and Mogami. Regarding steps (e) and (f), the Examiner relied upon Hidaka, at column 8, lines 38-50. However, the cited heavily doped regions 15a, 12b, 13b, 16b have the same conductivity type as the well in which these regions are formed, i.e. the referred to regions are well contact regions. Applicant cannot find any teaching or suggestion to dope the source/drain and gate electrode at a high and a low impurity concentration. Hidaka in no way teaches the claimed concept of doping CMOS at a high and low concentration, as claimed.

Mogami shows forming a gate electrode from undoped polysilicon layers, but does not remedy the deficiencies of Hidaka.

For at least the above reasons, claim 9 is believed clearly patentable over the cited references.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

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Respectfully submitted,

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